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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,042	01/22/2002	Steven R. Kunkel	ROC920010209US1	1375

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EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,042	KUNKEL ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,12-24 and 29-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,12-24 and 29-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed October 19, 2004.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 12, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 12, and 19, 29, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM as applied to claim 1, 12, and 19 above, and further in view of Parks (US. 6,594,736).

As per claims 1, 12, and 19, IBM teaches a method of managing cache in a shared memory multiple processor computer system:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least on of a plurality of processors (pages 1-2).

As per claims 1, 12, and 19 IBM teaches the claimed invention, but fails to teach executing, and purging the the cache line by the same processor.

Parks teaches migrating cache line (consider as purging cache lines) from the processor with modified data to another processor having copies of the related data (col. 2, lines 43-49).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the work of IBM because Parks teaches migrating cache line from the processor with modified data to another processor having copies of the related data in order to propagate the modification to all other caches.

As per claims 2, 13, and 20, IBM teaches the step of executing, by a processor, a cache purge instruction is performed after modifying the cache line by the processor (page 1).

As per claims 3, 14, and 21, IBM teaches wherein the cache line has a unique address (it is inherent in any cache system to have an address for each line).

As per claims 4, and 22, IBM teaches wherein the cache purge instruction updates all processors in the computer system (pages 1-2).

As per claims 5, and 23, IBM teaches wherein the cache purge instruction updates only an oldest cache line (page 2).

As per claims 6, and 24, IBM teaches wherein the cache purge instruction updates at least one level of cache (page 2).

As per claims 29, and 35, IBM teaches a method of managing cache in a shared memory multiple processor computer system, comprising:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least

one of a plurality of processors in the shared memory multiple processors (pages 1-2), wherein the cache purge instruction updates all caches in the computer system and marks a state of all updated cache line as shared (Page 2).

As per claims 29, and 35 IBM teaches the claimed invention, but fails to teach executing, and purging the cache line by the same processor.

Parks teaches migrating cache line (consider as purging cache lines) from the processor with modified data to another processor having copies of the related data (col. 2, lines 43-49).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the work of IBM because Parks teaches migrating cache line from the processor with modified data to another processor having copies of the related data in order to propagate the modification to all other caches.

4. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over IBM, Parks, and further in view of AAPA.

As per claim 30, IBM, and Parks teach a method of managing cache in a shared memory multiple processor computer system, comprising:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processors, wherein the cache purge instruction updates all caches in the computer system (page 2)

As per claim 30 IBM, and Parks teach the claimed invention, but fails to teach marking a state of all updated cache line as temporarily invalid. However, AAPA teaches when an entry in the cache is changed or modified, the directory temporary invalidates the respective directory entry corresponding to the cache line (page 8, paragraph 30, lines 6-8).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the work of IBM, and Parks because AAPA teaches temporarily invalidating a cache line in order to be over written if it is the oldest cache line.

5. Claims 15-16, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM, Parks, and further in view of Yates.

As per claims 15-16, and 34, IBM, Parks teach a computer system, comprising a shared memory and at least two processors wherein each processor is associated with at least one level of cache and wherein each processor, when executing a cache purge instruction and send the cache line to at least one other processor in the computer system to up date the at least one other processor (page 2).

As per claims 15-16, and 34 IBM, Parks teach the claimed invention, but fails to teach the cache purge instruction is referenced to at least five field and one of the at least five field indicates how the state of the updated cache(s) will be marked.

Yates teaches modification to multiprocessor, wherein there are five different modifications during updating data in caches of both processors (col. 30, lines 58-67).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the work of IBM, Parks because Yates teaches five different modifications during updating cache in order to show the status of cache for accessing.

6. Claims 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM, Parks, and further in view of Liu (US 5,210,848).

As per claims 31, and 36, IBM, Parks teach a method of managing cache in a shared memory multiple processor computer system:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least on of a plurality of processors (page 2).

As per claims 31-33, and 36-38 IBM, Parks teach the claimed invention, but fails to teach wherein the cache purge instruction updates only one cache at a designated processor of the plurality of processors then marks a state of the cache line updated as exclusive at the designated processor and marks a state of the cache line as temporarily invalid at the processor executing the instruction.

Liu teaches a multiprocessor system wherein updated cache lines are transferred to another processor, where the first processor mark that specific cache line as temporarily invalid and second processor marks it as exclusive so after data used by second processor it will be return to the first processor (claim 2).

Therefore, it would have been obvious to one having ordinary skill in the art to modify the work of IBM, Parks because Liu teaches two different mark status for a cache line while been used by two different processors at the same time in order to prevent modification without first processor permission.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 703-306-2758. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi
Examiner
Art Unit 2188

January 23, 2005

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER